

## ABSTRACT

An improved dynamic random access memory (DRAM) device with a capacitor having reduced current leakage from the dielectric layer, and materials and methods for fabricating the improved DRAM device are disclosed. The capacitor is formed using an  
5 oxygen anneal after a top conducting layer of the capacitor is formed.

W<sub>1</sub> W<sub>2</sub> W<sub>3</sub> W<sub>4</sub> W<sub>5</sub> W<sub>6</sub> W<sub>7</sub> W<sub>8</sub> W<sub>9</sub> W<sub>10</sub> W<sub>11</sub> W<sub>12</sub> W<sub>13</sub> W<sub>14</sub> W<sub>15</sub> W<sub>16</sub> W<sub>17</sub> W<sub>18</sub> W<sub>19</sub> W<sub>20</sub> W<sub>21</sub> W<sub>22</sub> W<sub>23</sub> W<sub>24</sub> W<sub>25</sub> W<sub>26</sub> W<sub>27</sub> W<sub>28</sub> W<sub>29</sub> W<sub>30</sub> W<sub>31</sub> W<sub>32</sub> W<sub>33</sub> W<sub>34</sub> W<sub>35</sub> W<sub>36</sub> W<sub>37</sub> W<sub>38</sub> W<sub>39</sub> W<sub>40</sub> W<sub>41</sub> W<sub>42</sub> W<sub>43</sub> W<sub>44</sub> W<sub>45</sub> W<sub>46</sub> W<sub>47</sub> W<sub>48</sub> W<sub>49</sub> W<sub>50</sub> W<sub>51</sub> W<sub>52</sub> W<sub>53</sub> W<sub>54</sub> W<sub>55</sub> W<sub>56</sub> W<sub>57</sub> W<sub>58</sub> W<sub>59</sub> W<sub>60</sub> W<sub>61</sub> W<sub>62</sub> W<sub>63</sub> W<sub>64</sub> W<sub>65</sub> W<sub>66</sub> W<sub>67</sub> W<sub>68</sub> W<sub>69</sub> W<sub>70</sub> W<sub>71</sub> W<sub>72</sub> W<sub>73</sub> W<sub>74</sub> W<sub>75</sub> W<sub>76</sub> W<sub>77</sub> W<sub>78</sub> W<sub>79</sub> W<sub>80</sub> W<sub>81</sub> W<sub>82</sub> W<sub>83</sub> W<sub>84</sub> W<sub>85</sub> W<sub>86</sub> W<sub>87</sub> W<sub>88</sub> W<sub>89</sub> W<sub>90</sub> W<sub>91</sub> W<sub>92</sub> W<sub>93</sub> W<sub>94</sub> W<sub>95</sub> W<sub>96</sub> W<sub>97</sub> W<sub>98</sub> W<sub>99</sub> W<sub>100</sub>